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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,902	07/24/2003	Hideyuki Otake	OKI.556	1200

20987 7590 10/27/2005

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EXAMINER

JEANGLAUDE, JEAN BRUNER

ART UNIT	PAPER NUMBER
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2819

DATE MAILED: 10/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/625,902

Applicant(s)

OTAKE, HIDEYUKI

Examiner

Jean B. Jeanglaude

Art Unit

2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on amendment filed on 9-27-05.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1,3 - 8,10-15,17-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,3 - 8,10-15,17-21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### Response To Amendments/Arguments

1. Applicant's arguments with respect to claims 1, 3 – 8, 10 – 15, 17 – 21 have been considered but are moot in view of the new ground(s) of rejection.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3, 5 – 6, 8, 10, 12, 13, 15, 17, 19, 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Brunolli et al. (US Patent Number 6,201,491).

4. Regarding claim 1, Brunolli et al. discloses a digital-to-analog converting circuit (figs. 3, 5) comprising: a first potential terminal ( $V_{CC}$ ) for supplying a first potential; a second potential terminal (the ground) for supplying a second potential; an output node (output) for outputting an analog signal (figs. 3, 5); a first resistor circuit (302, fig. 3; 902, fig. 5) having a plurality of first resistors connected in series between a first node and the output node through a plurality of first connecting points (figs. 3, 5); a first switching circuit ( $S9, \dots S12$ ) having a plurality of first switches each of which is connected directly to the first potential terminal ( $V_{CC}$ ), and to respective ones of the first connecting points and the first node (figs. 3, 5); a second resistor circuit (306, fig. 3; 906, fig. 5) having a plurality of second resistors connected in series between a second node and the output node through a plurality of second connecting points (figs. 3, 5); a

second switching circuit (S1,...,S4) having a plurality of second switches each of which is connected between directly to the second potential terminal (the ground), and to respective ones of the second connecting points and the second node (figs. 3, 5); and a control circuit (col. 6, lines 6 – 16) connected to the first and second switching circuits for controlling the first and second switches.

5. Regarding claim 3, Brunolli et al. discloses a digital-to-analog converting circuit (figs. 3, 5) wherein the second switching circuit (S1,...,S4) further has a second switch connected between the second potential terminal and the output node (figs. 3, 5).

6. Regarding claim 5, Brunolli et al. discloses a digital-to-analog converting circuit (figs. 3, 5) wherein the control circuit includes a first decoder for controlling the first switches and a second decoder for controlling the second switches (col. 6, lines 6 – 16).

7. Regarding claim 6, Brunolli et al. discloses a digital-to-analog converting circuit (figs. 3, 5) , wherein the first potential is a reference potential ( $V_{cc} = V_{ref}$ ) and the second potential is a ground potential (ground) (col. 6, lines 17, 18).

8. Regarding claim 8, Brunolli et al. discloses a digital-to-analog converting circuit (figs. 3, 5) comprising: a first potential terminal ( $V_{cc}$ ) supplying a first potential; a second potential terminal (the ground) supplying a second potential; an output node (the output) providing an analog signal; a plurality of first resistors (302, fig. 3; 902, fig. 5) connected in series between a first node and the output node, the first resistors being connected to each other at a plurality of first connecting points (figs. 3, 5); a plurality of first switches (S9,...S12) each of which is connected directly to the first potential terminal ( $V_{cc}$ ), and to respective ones of the first connecting points and the first node

Art Unit: 2819

(figs. 3, 5); a plurality of second resistors (306, fig. 3; 906, fig. 5) connected in series between a second node and the output node, the second resistors being connected to each other at a plurality of second connecting points (figs. 3, 5); a plurality of second switches (S1,...,S4) each of which is connected directly to the second potential terminal (the ground), and to respective one of the second connecting points and the second node (figs. 3, 5); and a control circuit connected to control the first and second switches (col. 6, lines 6 – 16).

9. Regarding claim 10, Brunolli et al. discloses a digital-to-analog converting circuit (figs. 3, 5) , further comprising an additional second switch (S1,..., S4) connected between the second potential terminal and the output node (figs. 3, 5).

10. Regarding claim 12, Brunolli et al. discloses a digital--to-analog converting circuit according to claim 8, wherein the control circuit includes a first decoder for controlling the first switches and a second decoder for controlling the second switches (col. 6, lines 6 – 16).

11. Regarding claim 13, Brunolli et al. discloses a digital-to-analog converting circuit (figs. 3, 5) , wherein the first potential is a reference potential ( $V_{cc}=V_{ref}$ ) and the second potential is a ground potential [ground] (col. 6, lines 17, 18).

12. Regarding claim 15, Brunolli et al. discloses a digital-to-analog converting circuit (figs. 3, 5) comprising: a first potential terminal ( $V_{cc}$ ) supplying a first potential; a second potential terminal (ground) supplying a second potential; an analog node providing an analog signal (the node at the output); a plurality of first resistors (302, fig. 3; 902, fig. 5) connected in series between a first node and the analog node through a plurality of first

Art Unit: 2819

connecting nodes (figs. 3, 5); a plurality of first switches (S9,...S12) each of which is connected directly to the first potential terminal, and to respective ones of the first connecting nodes and the first node (figs. 3, 5); a plurality of second resistors (306, fig. 3; 906, fig. 5) connected in series between a second node and the output node through a plurality of second connecting nodes (figs. 3, 5); a plurality of second switches (S1,...,S4) each of which is connected directly to the second potential terminal, and to respective ones of the second connecting nodes and the second node (figs. 3, 5); and a control circuit connected to control the first and second switches (col. 6, lines 6 – 16).

13. Regarding claim 17, Brunolli et al. discloses a digital-to-analog converting circuit (figs. 3, 5) further comprising an additional second switch (S1,...,S4) connected between the second potential terminal and the output node (figs. 3, 5).

14. Regarding claim 19, Brunolli et al. discloses a digital-to-analog converting circuit (figs. 3, 5), wherein the control circuit includes a first decoder for controlling the first switches and a second decoder for controlling the second switches (col. 6, lines 6 – 16).

15. Regarding claim 20, Brunolli et al. discloses a digital-to-analog converting circuit (figs. 3, 5), wherein the first potential is a reference potential ( $V_{cc}=V_{ref}$ ) and the second potential is a ground potential (col. 6, lines 17, 18).

### ***Claim Rejections - 35 USC § 103***

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

17. Claims 4, 11, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brunolli et al. (US Patent Number 6,201,491).

18. Regarding claims 4, 11, 18, Brunolli et al. disclose all the limitations as discussed above except the digital-to-analog converting circuit wherein the first switches are P-channel type MOS transistors and the second switches are N-channel type MOS transistors. However, P-MOS and N-MOS transistors are known to be an active device capable of switching components or elements in a circuitry. It is also known in the art that transistors are used as an alternative way to switch elements in a system. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that Brunolli et al. would perform the same function as the claimed invention.

19. Claims 7, 14, 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brunolli et al. (US Patent Number 6,201,491) in view Leung et al. (US Patent Number 6,400,300).

20. Regarding claims 7, 14, 21, Brunolli et al. discloses all the limitations as discussed above except the digital-to-analog converting circuit comprising an amplifier connected to the output node for amplifying analog signal. However, Leung et al., in a related field, discloses a DAC (figs. 1) comprising an amplifier (26) connected to the output node for amplifying analog signal (fig. 1). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Brunolli et al.'s system with that of Leung et al. in order to carry out conversion process.

### Conclusion

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. (See PTO-892).

22. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean B. Jeanglaude whose telephone number is 571-272-1804. The examiner can normally be reached on Monday - Friday 7:30 A. M. - 5:00 P.M..

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.



Art Unit: 2819

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Jean Bruner Jeanglaude

Primary Examiner

October 20, 2005